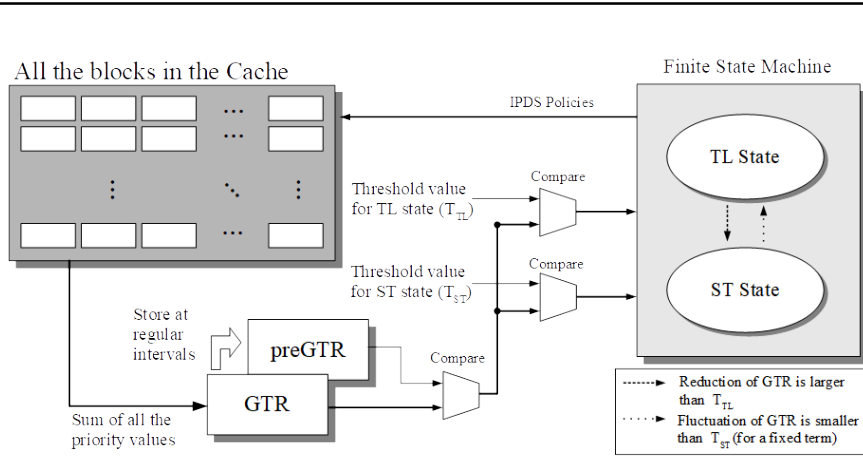
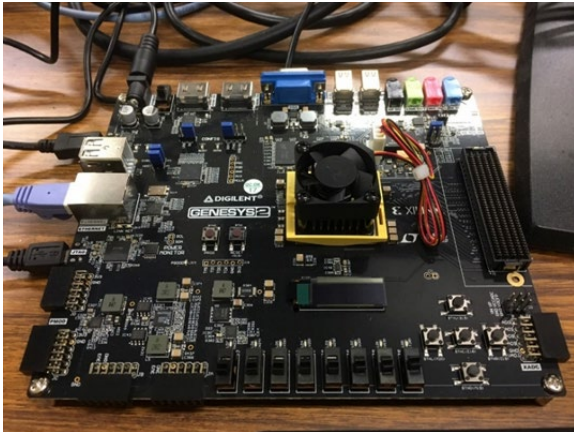


# Low-Power and High-Performance Computer Architecture

Associate Professor Jubeo Tada



## A Cache Replacement Policy with Considering Fluctuation Patterns of Total Priority Value



Implementation of a domain-specific RISC-V processor using FPGA board

### Content:

In recent years, computers are required to execute various fields of applications at high speed with low energy consumption. In addition, new devices are emerging one after another, such as three-dimensional integrated circuit stacking technology and FPGAs, so it is necessary to consider architectures that maximize the capabilities of these devices. On the other hand, computer performance relies heavily on components such as an arithmetic unit and a cache memory. Speeding up and reducing power consumption of these components achieve a higher performance of computers.

Tada lab is developing a domain-specific RISC-V processor suitable for executing specific applications such as artificial intelligence and data science. We are also conducting research on replacement algorithms to improve the performance of cache memory, and research on high performance and energy saving of processors using new semiconductor technologies such as 3DIC stacking technology. Appealing point:

Tada Lab is conducting research on computer architecture from both hardware and software sides. In recent years, we have been focusing on research on domain-specific RISC-V processors.

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